REMARKS

Claims 1-32 are currently pending in the subject application, and are presently under consideration. Claims 1-32 are rejected. Claims 2-7 and 13-17 have been indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 26 and 27 have been amended. Favorable reconsideration of the application is requested in view of the amendments and comments herein.

I. Rejection of Claims 1, 8-10, 12, 18-19, 24-32 under 35 U.S.C. 103

Claims 1, 8-10, 12, 18-19, 24-32 have been rejected under 35 U.S.C. 103 as being unpatentable over U.S. Patent Publication No. 2003/0195939 to Edirisooriya ("Edirisooriya ") in view of U.S. Patent No. 6,931,496 to Chen ("Chen"). Applicant traverses this rejection for the following reasons.

The Office Action dated May 23, 2006, contends that Edirisooriya discloses a system that includes a first node that includes data having an associated state, the associated state being a modified state, citing paragraph 22, lines 14-16, of Edirisooriya. In contrast to this contention, the disclosure at paragraph 22 of Edirisooriya relates to a processor 14 that sets or changes the state for an updated cache line within its cache to a modified state in response to an updated cache block being sent to such processor. In contrast to the contention in the Office Action, Edirisooriya does not teach or suggest the recited situation in which the first node includes data having an associated state, being in the modified state (which changes to an owner state), as recited in claim 1.

The Office Action refers to paragraph 19 of Edirisooriya, alleging a teaching of a second node that is operative to provide a non-migratory source broadcast request for the data, and that the second node is operative to receive the data from the first node and assign a shared state to an associated state of the data at the second node. In contrast to this contention, however, Edirisooriya does not teach or suggest that such a second node receives data from a first node having data in a modified state, as recited in claim 1. Moreover, Edirisooriya at paragraph 19 discloses a process that is associated with implementing a conditional read and invalidate request (CRIL).

As discussed at paragraph 17 of Edirisooriya, a CRIL request results in a transfer data between two caches in two situations:

> (a) two processors are attempting to gain exclusive control of a particular cache block and if one of the two processors receives a CRIL request holds that cache block in an owned state or a shared state, or
>
> (b) the processor issuing a CRIL request is attempting to gain exclusive control of the particular cache line a second processor holds a particular block in a modified state and is not currently attempting to gain control of the cache block.

That is, according to the teachings of Edirisooriya, the CRIL request is utilized to result in the transfer of data only in circumstances in which the processor is attempting to gain exclusive control of data. Thus, by definition, a CRIL request cannot correspond to a non-migratory source broadcast request for the data as recited in claim 1. Specifically, in claim 1, the non-migratory source broadcast request for the data results in a second node, which provided such request, receiving the data from the first node and assigning a shared state to an associated state of the data at the second node. In sharp contrast, the CRIL request is utilized to gain exclusive control of the data and would not correspond to a shared state.

The Office Action admits that Edirisooriya fails to teach that the first node is operative, in response to the non-migratory source broadcast request, to provide the data to the second node and to transition the associated state of the data at the first node from a modified state to an owner state without updating memory. Additionally, applicant respectfully points the Examiner that the reason that Edirisooriya fails to teach such claimed subject matter is that, as discussed above, the CRIL request is intended to get the data for exclusive control by the requesting processor. Accordingly, such state transitions at node that provides the requested data (*e.g.*, a transition from a modified state to an owner state without updating memory as recited by claim 1) is not suggested in the teachings of Edirisooriya.

The Office Action also relies on Chen; however, Chen fails to make up for the deficiencies of Edirisooriya noted above. The Office Action generally cites Col. 5, lines 5 – 10 of Chen, which describes two various states for an external L3 cache line. The Office Action also cites Col. 5, lines 36 – 42 of Chen, which describes local access commands that can be asserted by a local processor via the system bust. Specifically, the latter cited portions of Chen relate to a BRIL(hitm#) command and to a BIL command. As mentioned above, these commands are local access commands that are implemented within a given node of the

system for accessing a shared L3 cache. The particular states identified above thus correspond to the state of data in a single local cache (i.e., an external L3 cache of a given node) that may be accessed by different processors of such node. Coherency of the external L3 cache is maintained by a DSM controller. The states of the data in the L3 cache of Chen identified in the Office Action do not correspond to states of different nodes that might be requesting data. Applicant respectfully points the Examiner to Col. 6, line 34, through Col. 7, line 17, of Chen, relating to certain functionality that can be carried out within the local node 11 relative to the cache states identified in the Office Action.

Applicant submits that one of ordinary skill in the art would not be motivated to modify the system of Edirisooriya based on the teachings of Chen since each of the respective teachings taken individually, as well as in combination fail, to teach or suggest the subject matter recited in claim 1. For instance, as discussed above, Chen does not teach or suggest a node (the first node of claim 1) that provides the data in response to a non-migratory source broadcast request transitions its state from the modified state to the owner state without updating memory, as recited in claim 1. Instead as discussed above, Chen teaches that it is the external L3 cache itself, residing within a local node having multiple processors, which undergoes state transitions. Applicant further submits that the state transitions disclosed and relied on in the Office Action do not correspond to the state transitions and other functional relationships recited in claim 1. Thus, even if the respective teachings are combined and can somehow efficiently solve an access deadlock problem, as suggested in the Office Action, the resulting system would not make claim 1 obvious for the reasons stated above. For these reasons, applicant respectfully requests reconsideration and allowance of claim 1 and claims 2-11, which that depend from claim 1.

Regarding claim 8, the Office Action contends that Chen discloses that the first node is operative in response to a non-migratory source broadcast request to provide a shared data response to the second node, citing Col. 6, lines 1 – 6 of Chen. However, Col. 6, lines 1 – 6 of Chen discloses that "the ROF command is issued to change the state of local memory line of the remote node, where the specified data is stored from shared into home on the condition that the state of the cache line of the local node where the data is stored has changed from fresh to stale." This is in sharp contrast to what is recited in claim 8, in which the first node is operative in response to the non-migratory source broadcast request to provide a shared data response to the second node. Similar to as discussed above with respect to the rejection of claim 1, the rejection appears to be based on teachings of Chen in which the only object or

component with a cache state corresponds to an external cache within the local node. Moreover, the ROF command is utilized to cause another node to abandon the data in the cache line, and does not correspond to the shared data response recited in claim 8. See Chen at Col. 9, lines 5 – 7. Applicant submits that the reliance on Chen relative to claim 8 appears without merit in view of the teachings of Chen. Reconsideration and allowance of claim 8 are respectfully requested.

The Office Action contends that Chen discloses the subject matter recited in claim 10, citing Col. 7, lines 55 – 61 of Chen. This contention appears improper in view of this and other teachings of Chen. Specifically, the cited section of Chen and Chen more generally does not describe the interrelationship of data requests and responses when more than two nodes may be present. Claim 10 recites "at least one other node...," which at least implicitly would be different from the first node and the second node recited claim 1 from which claim 10 depends. The cited section of Chen does not relate to any such at least one other node nor does it identify any teaching or suggestion might imply the claimed interrelationships where at least one other node provided a non-data response to the second node in response to the non-migratory source broadcast request from the second node. Instead, the cited section of Chen relates generally to a remote access command to read a copy of data and to read an exclusive copy of data if data in the external L3 cache of a processor 112 is in one of the dirty-only or dirty-shared states. For these reasons reconsideration and allowance of claim 10 are respectfully requested.

Claim 12 has been rejected for the same rationale as the rejection of claim 1. Applicant submits that the recitations of claim 12 are further distinguishable over the combination of Edirisooriya and Chen. For example, in claim 12, it is explicitly recited that a processor node has a cache line in a modified state and a second processor also has a second processor node cache line at an associated state, the second processor node provides a non-migratory source broadcast read request for the data. In response to receiving the data, the associated state of the second processor nodes cache lines is assigned a shared state, further distinguishing the CRIL request which it is utilized to obtain exclusive control over the requested data according to the teachings of Edirisooriya. Moreover, in claim 12, each of the first and second processor nodes includes cache lines having respective states, which is a marked distinction when compared to the use of the external L3 cache taught by Chen. Thus, as discussed above with respect to claim 1 there is no teaching or motivation based on which one of ordinary skill in the art would reasonably be able to modify Edirisooriya based on the

teachings of Chen to provide the subject matter recited in claim 12. For these reasons reconsideration and allowance of claim 12 as well as claims 13 – 20 depending therefrom, are respectfully requested.

Applicant submits that claim 19 is further allowable for at least the reasons stated above with respect to claim 10.

Claim 24 is written in means plus function format and is allowable for at least those reasons stated above with respect to claim 1.

Claim 25 should be allowable for the similar reasons to claim 2, which was indicated as containing allowable subject matter. Specifically, claim 25 depends on claim 24 and recites means for broadcasting a migratory read request for data. Applicant respectfully requests that the Examiner reevaluate claim 25 in view of the art of record based on which applicant respectfully submits should result in the allowance of claim 25.

Claims 26 and 27 have been amended to depend from claim 25 to correct typographical errors. Applicant submits that the further means for selecting one of the XREADM request or the XREADN request is not taught or suggested in Chen as suggested in the Office Action, such that claim 26 should be allowed.

Regarding claim 27, Applicant respectfully submits that Chen does not teach or suggest any structure to be able to predictably selecting either the XREADM request or the XREADN request. Accordingly, applicant respectfully requests reconsideration and allowance of amended claim 27.

Claim 28 is allowable over the art of record for at least those reasons stated above with respect to claim 1.

Claim 29 depends from claim 28, and similar to claim 25, recites a method in which a migratory request for data is broadcast from the first node and an ownership data response from the second node to the first node is provided in response to the migratory request. The state of the data at the second node (a received migratory request) transitions from a modified state to an invalid state in response to the migratory request. The state of the data at the first node transitions to a dirty state in response to receiving the ownership data response from the second node. Applicant respectfully submits that the teachings of Chen fails to teach the types of request between nodes that accompany the transition the state associated with the data at the first and second nodes as recited in claim 29. For at these reasons, reconsideration and allowance of claim 29 are respectfully requested.

Claims 30 and 31 depend from claim 29 and should be allowed for at least those reasons stated above with respect to claims 28 and 29.

Regarding claim 32, the Office Action relies on the rationale that was utilized in the rejection of claim 1. However, similar to as discussed above with respect to claim 12 and 1, the purported combination of Edirisooriya and Chen would not make it obvious to a person of ordinary skill in the art to make a computer system as recited in claim 32. For example, neither Chen nor Edirisooriya teach or suggest the use of a cache coherency protocol that is operative for migration of data to a cache associated with a source processor from a cache associated with a target processor when a migratory request is issued from the source processor and in which the protocol is operative to prevent migration of data to the cache associated with the source processor from the cache of the target processor when a non-migratory request is issued from the source processor. Applicant respectfully submits that this combination of features for cache coherency protocol in the computer system of claim 32 is not taught or suggested in the art of record such that claim 32 should be allowed.

II. **Rejection of Claims 11 and 20-23 under 35 U.S.C. 103**

Claims 11 and 20-23 have been rejected under 35 U.S.C. 103 as being unpatentable over Edirisooriya in view of Chen and further in view of U.S. Patent No. 6,484,240 to Cypher ("Cypher"). Applicant traverses this rejection for the following reasons.

Claim 11 depends from claim 1 and is allowable for at least the reasons discussed above with respect to claim 1. The Office Action rejects claim 11 as being unpatentable over Edirisooriya in view of Chen and further of U.S. Patent No. 6,484,240 to Cypher. However, Cypher fails to make up for the aforementioned deficiencies relative to the combination of Edirisooriya and Chen. Accordingly, reconsideration and allowance of claim 11 is respectfully requested.

Similarly, claim 20 depends from claim 12 and is allowable for at least the reasons stated above with respect to claim 12.

Claim 21 has been rejected based on the rationale applied in the Office Action to claims 1 and 11. Claim 21 recites a source processor that is operative to issue a selected one of a non-migratory source broadcast request for data and a migratory source broadcast request for data. The target processor is programmed to respond to the non-migratory source broadcast request by providing a shared data response to the source processor and by transitioning the state of target processor from the modified state to the owner state without

updating the memory. The target processor is also programmed to respond to the migratory source broadcast request for the data by providing the ownership data response to the source processor and by transitioning the associated state of the target processor cache line from the modified state to the invalid state. As discussed above with respect to claim 13, and as discussed above with respect to claim 1, the combination of Edirisooriya and Chen, or even if combined with Cypher, fails to teach or suggest the computer system recited in claim 21, in which the source processor having an associated source processor cache is operative to issue a selected one of a non-migratory source broadcast request or a migratory source broadcast request for the data that is stored in the memory and in a modified state of the target processor. As discussed in greater detail above with respect to claim 1, neither Chen nor Edirisooriya teach or suggest implementing the particular state transitions associated with providing a response to the particular request issued by the source processor as recited in claim 21. For these reasons claim 21 is patentable and its allowance is respectfully requested.

Claim 22 has been rejected based on the teaching of Chen, specifically at Col. 6, line 58, through Col. 7, line 17, and Col. 7, line 49, to Col. 8, line 3. Even the cited section of Chen at Col. 7, lines 13 – 17 specifically teaches that to obtain an exclusive copy of data, the processor asserts a BRIL or BIL command. Thus, the commands identified in the Office Action to reject to claim 1, namely the BRIL (hitm#) and the BIL, do not result in the issuing of such commands for assigning a shared state to the state of the cache line in response to receiving data from the target processor. Instead, the commands being relied upon result in the processor that asserts such command having exclusive ownership, not transitioning to shared state as recited in claim 22. Applicant respectfully requests reconsideration and allowance of claim 22.

The Office Action contends that Chen discloses the additional recitation of claim 23, citing Chen at Col. 7, lines 49 – 61 and Col. 8, lines 52 – 67. In contrast to the contention in the Office Action, the cited sections of Chen disclose transition such as from dirty-only or dirty-shared to fresh and changing the state of a cache line from dirty-only or dirty-shared to void (Col. 7, lines 49 – 61). The other section relied on to reject claim 23 relates to a transition from clean dirty-shared or dirty-only to stale and from stale to void. In sharp contrast to such teachings in Chen, claim 23 recites that the processor stores the data in the source processor cache line and assigns a dirty state to the associated state of the data in response to receiving an ownership data response from the target processor. As discussed above with respect to claim 12, Applicant further points out that, in claim 23, it is the source

processor that comprises an associated source processor cache having a source processor cache line. Whereas, the respective cache disclosed in Chen relates to an external L3 cache within a given node, which Chen teaches does not correspond to a source processor cache but to an external cache in which cache coherency is maintained by the DSM controller for each of the respective nodes. Thus, for these reasons and the reasons stated above with respect to claim 21, applicant respectfully requests reconsideration and allowance of claim 23.

III. ALLOWABLE SUBJECT MATTER

Applicant appreciates the indication that claims 2-7 and 13-17 contain allowable subject matter, and would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

IV. CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the present application is in condition for allowance. Applicant respectfully requests reconsideration of this application and that the application be passed to issue.

Should the Examiner have any questions concerning this paper, the Examiner is invited and encouraged to contact Applicant's undersigned attorney at (216) 621-2234, Ext. 106.

No additional fees should be due for this response. In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to Deposit Account No. 08-2025.

Respectfully submitted,

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